# DIGITAL DELAY LOCKED LOOP WITH EXTENDED PHASE CAPTURE RANGE

## Abstract

A digital delay locked loop uses a delay array to delay an input signal by an amount indicated by a delay code. A phase of the resulting delayed signal is compared to a corresponding phase of the input signal, and dependent on the comparison, the delay code is updated to indicate whether the delay array needs to provide more delay or less delay. The digital delay locked loop also uses a detection circuit that monitors for a predetermined condition of the delay code. In response to detection of the predetermined condition, the delay code is automatically reset to a value different than a value of the delay code present at a previous reset or initial startup of the digital delay locked loop.

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